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A Low Power Clock Gating Based On Look Ahead Clock Gating

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ABSTRACT: The low power look ahead clock gating method combines the previously three methods. The major power consumers in computing and consumers electronics products is the systems clock signal, typically responsible for 30% to 70% of the total switching power consumption. Several techniques to reduce the power have been developed of which clock gating is predominant. This look ahead clock gating computes the clock enabling signals of each flip flop one cycle ahead of time, based on the present cycle data of those flip flops on which it depends. It avoids the tight timing constraints of auto gated and data driven by allotting a full clock cycle for the computation of the enabling signals and their propogation. A low power look ahead clock gating model is presented which is based on the auto gated flip flop. The comparison between the look ahead, data driven clock gating is done. The result shows the look ahead consumes 16nw while the data driven consumes 24nw power which is greater than the proposed look ahead clock gating. This clock gating is very useful for reducing the power consumed by digital systems. Power consumption plays an important role in any integrated circuit and is listed as one of the top three challenges in international technology roadmap for semiconductor.

KEYWORDS: Power reduction, clock gating.

I.INTRODUCTION

In the earlier period, the VLSI designers were more bent towards the performance and area of the circuits Reliability and cost also gained core importance whereas power consumption was a peripheral consideration. In recent years however a power being given equal importance in comparison to area and speed. As technology scales down, short circuit and leakage power becomes comparable to dynamic power dissipation. Consequently, the identification and modelling of different leakage and switching components is very important for the estimation and reduction of power consumption especially for high speed and low power applications. Clock gating is predominant to reduce the power consumption. With clock gating, the clock signals are ANDed with explicitly predefined enabling signals, clock gating is employed at all levels, system architecture, block design, logic design and gates. Previously, three gating methods are known[2], first is the synthesis based, deriving clock enabling signals based on the logic of the underlying system. It unfortunately leaves the majority of the clock pulses driving the flip flop redundant. A data driven method stops most of those and yields higher power savings, but its implementation is complex and application dependent. A third method called auto gated flip flop is simple but yields relatively small power savings. Synthesis based clock gating is the most widely used method by EDA tools. Clock enabling signals are very well understood [1] the system level and thus can effectively be defined and capture the periods where functional blocks and modules do not need to be clocked. Those are later being automatically synthesized into clock enabling signals are manually added for every flip flop as a part of a design methodology still, when modules at a high and gate level are clocked, the state transistor of their underlying flip flops depend on the data being processed. It is important to note that the entire power consumed by a systems stems from the periods where modules clocked signals are enabled. The data driven clocked gating method was proposed to address the flip flops redundancy. The clock signal driving a flip flop is disabled when the flip flops state is not subject to change in the next clock cycle. In an attempt to reduce the overhead of the gating logic, several flip flops are driven by the same clock signal, generated by ORing the enabling signals of the individual flip flops. As consumers continue to demand more functionality in smaller, more energy efficient devices, power optimization rules a hardware designer life.

The clock signals have been a great source of power dissipation because of high frequency and load. Clock signals do not perform any computation and mainly used for synchronization. Hence these signals are not carrying any information. So, by using clock gating one can save power by reducing unnecessary clock activities inside the gated module. In many applications, the power consumption of the IC clock system is one of the main sources of chip power dissipation. To address the redundancy from the synthesis based, a data driven clock gating is proposed for flip flops.

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There the clock signals driving a flip flop is disabled when the flip flops state is not subject to change in the next clock cycle. The data driven gating suffers from a very short time window where the gating circuitry can properly work. The delay of the XOR, OR, latch and the AND gater must not exceed the set up time of the flip flop. Another difficulty of data driven clock gating is its design methodology. The low power look ahead clock gating method combines the previously three methods. The major dynamic power consumers in computing and consumers electronics products is the systems clock signal, typically responsible for 30% to 70% of the total dynamically switching power consumption. Several techniques to reduce the dynamic power have been developed of which clock gating is predominant. This look ahead clock gating computes the clock enabling signals of each flip flop one cycle ahead of time, based on the present cycle data of those flip flops on which it depends. It avoids the tight timing constraints of auto gated and data driven by allotting a full clock cycle for the computation of the enabling signals and their propogation. A low power look ahead clock gating model is presented which is based on the auto gated flip flop. The comparison between the look ahead , data driven clock gating and the power gating is done. The result shows the look ahead consumes 16nw while the data driven consumes 24nw power which is greater than the proposed look ahead clock gating. This clock gating is very useful for reducing the power consumed by digital systems. Power consumption plays an important role in any integrated circuit and is listed as one of the top three challenges in international technology roadmap for semiconductor. The rest of the paper discusses the clock gating, designing of the data driven clock gating and the look ahead clock gating and the power comparison between the above both and the simulation results.

II.RELATED WORK

As part of related work, here have exploring and learning various terminologies and techniques related to VLSI. As this topic is on Gating technique, i.e. clock gating so the terms like clock gating, clock networks and look ahead clock gating, power gating and the previous methods, technique related to this are needed to get explored. one of the major power consumers in computing and consumer electronics products is the system's clock signal, typically responsible for 30% to 70% of the total dynamic (switching) power consumption. Several techniques to reduce the dynamic power have been developed.

Previously, synthesis based gating still leaves a large amount of redundant clock pulses. Secondly, the data driven gating aims to disable these. To reduce the hardware overhead involved, flip flops are grouped so that they share a common clock enabling signal. The question of what is the group size maximizing the power savings is answered and which flip flops should be placed in a group to maximize the power reduction. Consequently, the switching of a significant portion of the system's clock load is redundant, but consumes most of its power. Data driven clock gating is reducing the total power consumption of VLSI chips by 20%. There, flip flops are grouped and share a common clock signal. Finding the optimal clusters is the key for maximizing the power savings.

In this, a new pulse triggered flip flop in look ahead clock gating is presented in which power dissipation is reduced by deactivating the clock signal on both master and slave latches when there are no data transitions. The new circuit overcomes the clock duty cycle constraints of previously proposed gated flip flops. The reason behind selecting this paper is that it proposes a power reduction technique. This power saving is a need of today. To do this, there are various ways. Several techniques to reduce the power have been developed, of which clock gating is predominant. This paper proposes a clock gating method that is "A low power look ahead based on auto gated flip flops". Look ahead clock gating finds the clock enabling signals of each FF one cycle ahead of time, based on information of the present data of flip flop on which it depends. Look ahead clock gating takes auto gated flip flop a leap forward

III.EXISTING SYSTEM DATA DRIVEN CLOCK GATING

Data driven clock gating block diagram and circuit diagram is shown in the fig 1. This data driven clock gating causes area and power overhead. The power consumption could be reduced by using clock gating technique. This data driven clock gating signals having activity to enable the clock signals. So, the flip flops and the latches are to be enabled by using the gate signals. The outputs from the XOR gates are ORed to give the combination of output joint gate signals from the flip flops and then latched to avoid the glitches presented in the specified units. The clock of the flip flop can be disabled in the next cycle by XORing its output with the present input data that will appear at its output in the next cycle. The data driven gating suffers from a very short time window where the gating circuitry can properly work[5]. The cumulative delay of the XOR, OR, latch and the AND gater must not exceed the setup time of the flip flop. Such constraints may exclude five percent to ten percent of the flip flops from being gated due to their presence on timing critical paths. The exclusion percentage increases with the increase of critical paths, a situation occurring by down sizing or turning the transistors of non critical path to high threshold voltage for future power savings.

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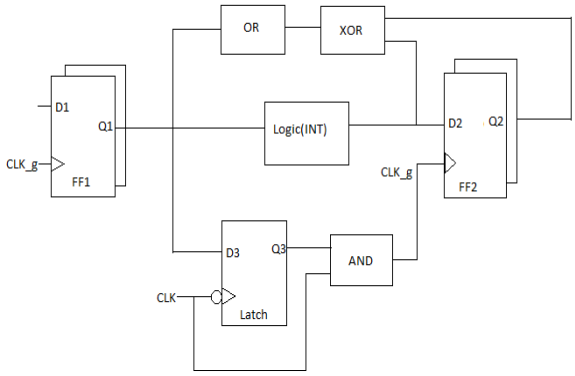

Fig. 1 Data driven clock gating Block Diagram

IV.PROPOSED SYSTEM LOOK AHEAD CLOCK GATING

The look ahead clock gating block diagram is shown in fig 2. It is based on the auto gated flip flop in the sense it uses the auto gated output part. Flip flops have their content modification solely either at the rising or falling fringe of the modify signal. But, once the rising or falling fringe of the modify signal, the flip flops content remains constant even though the input modification. In a very typical D flip flop[4], the clock signal perpetually flows into the D flip flop no matter whether or not the input changes or not. A part of the clock energy is consumed by the interior clock buffer to manage the transmission gates unnecessarily. Hence, if the input of the flip flop is the image of its output, the shift of the clock will be suppressed to conserve power.

The look ahead path and pipelining to eliminate the carry delay. The look ahead clock gating block consists of Enhanced auto gated symbol for master and the slave blocks. This could be used as a look ahead structure for reducing the timing constraints of the each block. The enhanced auto gated flip flops could be having the related use of the sectional circuits from the each and every input. The output from the flip flop as Q and X could be input of the logic block and the continuous input to another block. The XOR and the OR gated logic could be used as a leap forward approach for the input signal. The clock and the gated clock also given to the logic and then it will be adopted as a signal from the each block of the architecture. The rising and the falling edge of the clock pulses enables the clock load from the switching. The output from the flip flop could be given to the logic as well as the gated signal as for the output of the next level logic. The gated signal clock pulses also to be the path recognize of the master slave of the enhanced auto gated logic. This logic has been given to the next level of the flip flop for automatic process of the gate as general signals from the input. Then the output of the flip flop could be given to the clock gated signal and the clock enabling signals to give the final output. This gives the timing constraints path of the look ahead clock signal from the inputs.
The look ahead clock gating overcomes the drawbacks of the auto gated flip flops in the tight timing constraints from the clock pulses which is not enabled in the gated signal. The structural details from the signals where it could not be recognize in the rising and the falling edges of the clock pulses. During the computation path the setup time and the holding timing can also to enable in the path of all input pulses from the master slave blocks The basic circuit used for look ahead clock gating is auto gated flip flops. This look ahead clock gating takes the auto gated flip flop a leap forward, addressing three goals; Stopping the clock pulse also in the master latch, making it applicable for large and general designs and avoiding the tight timing constraints. Look ahead is based on using the XOR output to generate the clock enabling signals of other flip flops in the system, whose data depend on that flip flop. Here the look ahead clock gating includes the flip flops, XOR gate, AND latch, OR gate and the logic is inverter.

The look ahead clock gating circuit is design in the Tanner EDA tool version 13.00. This look ahead clock gating with inverter logic is designed and simulated. Then the data driven is designed and simulated and compared with the look ahead clock gating. It shows that the look ahead clock gating consumes less power than the previous data driven clock gating technique. This is design in a 22nm technology in a tanner EDA tool 13.00 version. The simulation results for all existing and proposed technique were obtained, in a 22nm technology at room temperature using Tanner EDA tools 13.00 over the supply voltage and frequency. Table I shows the power comparison results for the data driven clock gating and look ahead clock gating. It shows the data driven clock gating consumes 24nw and the look ahead

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clock gating consumes 16nw which is less than the data driven clock. This clock gating is a popular technique used in many synchronous circuits for reducing power consumption. Clock gating saves power by adding more logic to a circuit to prune the clock tree. Pruning the clock disables portions of the circuitry so that the flip flops in them do not have to switch states. Switching states consumes power. A flip flop finds out that its clock can be disabled in the next cycle by XORing its output with the present input data that will appear at its output in the next cycle. Here the output of XOR gate are OR to generate a gating signal for flip flops, which is then latched to avoid glitches. When not being switched, the switching power consumption goes to zero, and only leakage currents are incurred. Here clock gating works by taking the enable conditions attached to registers, and uses them to gate the clocks. Therefore, it is imperative that a design must contain these enable conditions in order to use and benefit from clock gating. This clock gating process can also save significant die area as well as power. This clock gating is a popular technique used in many synchronous circuits for reducing power consumption.

In general, finding sets of flip flops that minimize the number of redundant clock pulses is not enough to maximize power savings. Grouping must account for the on-die locations of flip flops and gaters, which affect the power consumption due to the capacitive loads resulting from their connections. The physical location of flip flops affect also the delay, and it is therefore desirable for flip flops driven jointly by the same clock gater,[4] to be placed in proximity of each other. Using a flip flop for gating is a considerable overhead that will consume power of its own. This can significantly be reduced by gating flip flop since the flip flop is oppositely clocked and its data is sampled at the clock falling edge, its clock enabling must be negated. In look ahead clock gating, also a flip flop is an ordinary flip flop where the internal XOR gate is connected. Real implementation may require long wires to generate the clock enabling signals, so the grace of a full cycle is a big relief.

Clock gating, clock gating limits the clock from being given to every register or flip flops in the processor. In clock gating the gated areas will still be provided with bias power. In this the Tanner tool is used for designing the circuit and for taking their simulation. Other intelligent clock gating techniques are used to minimize the activity portions of the design that do not contribute to the design output for that clock cycle. Clock gating reduces power by preventing logic not used in a given clock cycle from toggling in the clock cycle. Additionally, it prevents the clocks to the flip flops in cases where the clocking either does not produce new data or flip flop outputs are not used by subsequent logic in a given clock cycle. These gating techniques reduces the dynamic and total power consumption. Clock signal is one of the main sources of chip power, high switching activity, heavy capacitive loading of the clock network. Mostly the latch based circuits are used. The low power circuits are most powerful in the circuit as the scaling increase the leakage powers increases. So far, removing these kinds of leakages there are many kinds of power gating techniques and to provide a better power efficiency. The process of scaling techniques to nano meter regime has resulted in a rapid increase in leakage power dissipation. Here, the clock gate which could be enables the clock signal from the clock distribution network. This technique could be activating the clock which is needed for the operation of the circuit. The unnecessary clock signals are not activated during the clock gating. This saves the dynamic power of the circuit. The auto gated flip flops which are to be using clock gating technique for only small power consumption. The implementation of this technique could be much more difficult. The clock enabling signal from the each flip flop defines the more power dissipation included the gated logic. This circuit depends on the application for the device and it cannot be added as a delay based component. Circuit simulation with inclusion of parasitics show that sensible power dissipation reduction is possible if input signal has reduced switching activity. In a synchronous system, a flip flop is triggered by a certain directional transition of a clock signal. For the clock to be another signal rather than the master clock, it must offer the same directional transition to trigger the flip flop and it must be in step with the master clock. This look ahead clock gating has been shown[5] to be very useful in reducing the clock switching power than the data driven clock gating. The look ahead clock gating having the advantages that it stops the clock pulses also in the master latch, second making it applicable for large and general designs and third avoiding the tight timing constraints. Clock gating is being used for reduction of power consumption in low power circuits for quite a while now. Adaptive clock gating is most rigorous of them all. Since gating the clock signals involve additional circuitry there exists a tradeoff between the additional number of gates and the total power consumption of gated clock.

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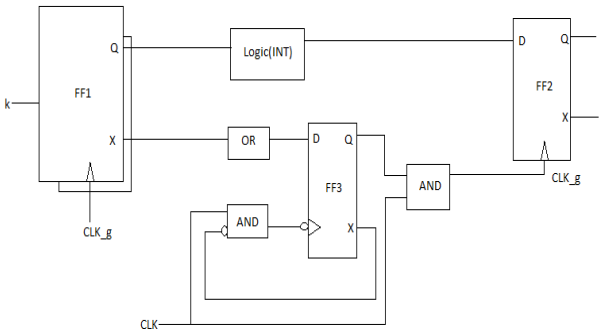

Fig. 2 Look ahead clock gating Block Diagram

V.IMPLEMENTATION

The following figures shows the implementation part for the data driven clock gating and look ahead clock gating methods and their waveforms. The below circuit diagrams are designed in the tanner EDA 13.00 version. The schematic in the S-Edit of the tanner and the waveforms in the W-Edit.

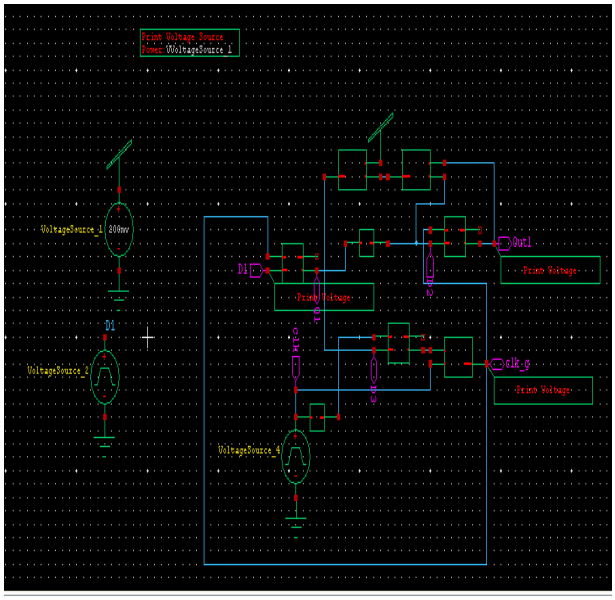

Fig.3 Data driven clock gating circuit

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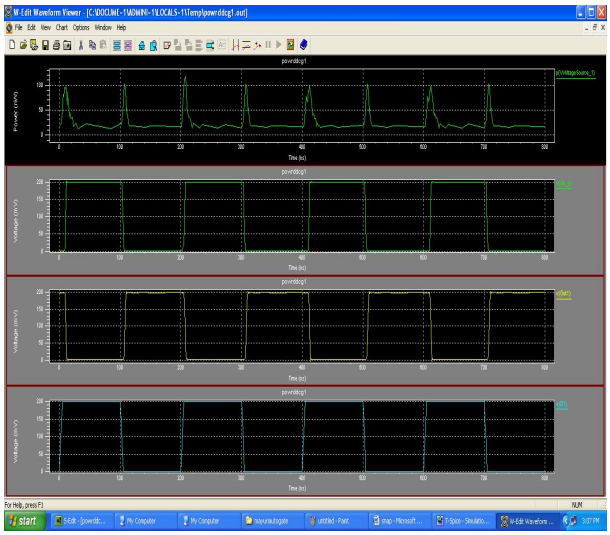

Fig. 4 Data driven clock gating waveforms.

Data driven clock gating circuit diagram implementation is shown in the above figure 3 and its respective waveforms in figure 4. This data driven clock gating causes area and power overhead. The power consumption could be reduced by using clock gating technique[1]. This data driven clock gating signals having activity to enable the clock signals. So, the flip flops and the latches are to be enabled by using the gate signals. The outputs from the XOR gates are ORed to give the combination of output joint gate signals from the flip flops and then latched to avoid the glitches presented in the specified units. The clock of the flip flop can be disabled in the next cycle by XORing its output with the present input data that will appear at its output in the next cycle. The data driven gating suffers from a very short time window where the gating circuitry can properly work. The cumulative delay of the XOR, OR, latch and the AND gater must not exceed the setup time of the flip flop. Such constraints may exclude five percent to ten percent of the flip flops from being gated due to their presence on timing critical paths. The exclusion percentage increases with the increase of critical paths, a situation occurring by down sizing or turning the transistors of non critical path to high threshold voltage for future power savings.

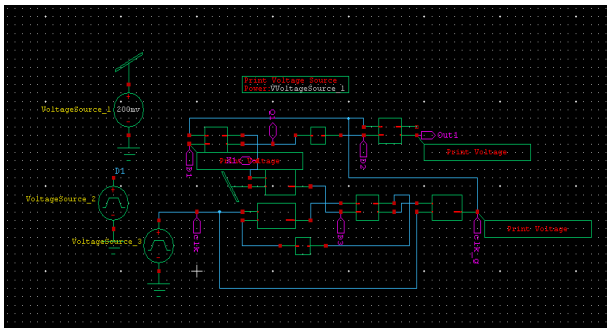

Fig. 5 Look ahead clock gating circuit.

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Specific clock gating cells are required in library to be utilised by the synthesis tools. Availability of clock gating cells and automatic insertion by the EDA tools makes it simpler method of low power technique. Advantage of this method is that clock gating does not require modifications to RTL description.Look ahead clock gating takes auto gated flip flop a leap forward, addressing three goals. Stopping the clock pulse also in the master latch, making it applicable for large and general designs and avoiding the tight timing constraints. Look ahead cock gating is based on using the XOR output to generate clock enabling signals of other flip flops in the system, whose data depend on that flip flop.

Fig. 6 Look ahead clock gating waveforms.

The look ahead clock gating circuit diagram implementation is illustrated and shown in fig 5 and its waveform is shown in fig 6. The two flip flops are there the first is source flip flop and the second is the target flip flop. The logic driving a target flip flop does not have an input externally of the block. X(D) denote the set of the XOR outputs of the source flip flops, and denoted by Q (D) the set of their corresponding outputs. The source flip flops can be found by a traversal of the logic path from D back to Q(D). Figure 6 shows the waveforms for look ahead clock gating circuit. The waveform shows input, output and the power waveforms. Clock enabling signals are very well understood at the system level and thus can effectively be defined and capture the periods where functional blocks and modules do not need to be clocked. Those are later being automatically synthesized into clock enabling signals at the gate level. In many cases, clock enabling signals are manually added for every flip flop as a part of a design methodology. Still, when modules at a high and gate level are clocked, the state transitions of their underlying flip flops depend on the data a being processed.

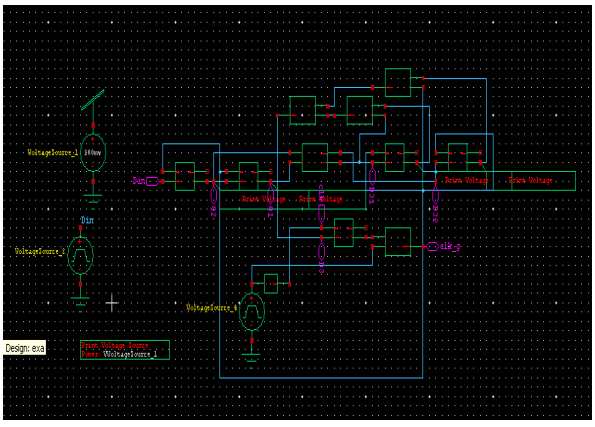

Fig. 7 Look ahead clock gating with adder implementation.

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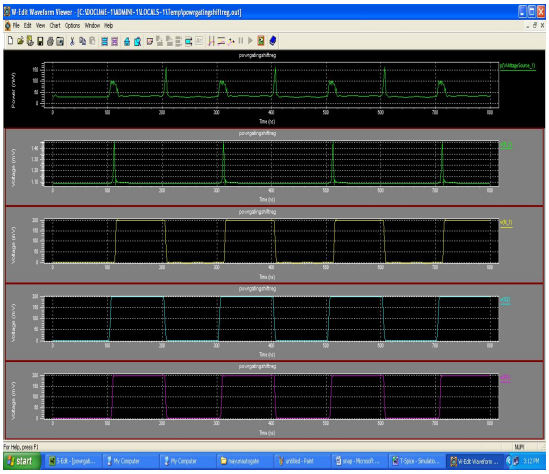

Fig. 8 Look ahead clock gating with adder waveforms.

Fig 7 shows the look ahead clock gating with adder circuit example and its respective waveforms in fig 8. Clock enabling signals are usually introduced by designers during the system and clock design phases, where the inter-dependencies of the various functions are well understood. In contrast, it is very difficult to define such signals in the gate level, especially in control logic, since the inter-dependencies among the states of the various flip flops depend on automatically synthesized logic

VI. SIMULATION RESULTS AND DISCUSSION

The simulation results for the existing and proposed techniques were obtained and shown, in a 22nm technology at room temperature using Tanner EDA tools 13.00 over the supply voltage 200mv and frequency. Following table I shows the power comparison results for the data driven clock gating and look ahead clock gating. Table shows that data driven clock gating consumes 24nw and the look ahead clock gating consumes 16nw which is less than the data driven clock gating. With the more reduction in the power consumed, the proposed technique is beneficial.

TABLE I Power Consumption for Gating Techniques

Design Name	Supply Voltage	Power Consumed
Data Driven Clock Gating	200mv	24nw
Look Ahead Clock Gating	200mv	16nw

As this topic is on the low power, so here have brought the technique called “A low power look ahead clock gating based on auto gated flip flops”. This look ahead clock gating finds the clock enabling signals of each flip flop one cycle ahead of time, based on information of the present data of flip flop on which it depends. This look ahead clock gating takes the auto gated flip flop a leap forward. It deals with three goals; taking the clock pulse in the master latch also, making it practical for large and general designs and avoiding the issues of timing constraints. The main objective of look ahead is to reduce the power consumption and this technique is considerably simpler.

VII.CONCLUSION

In this paper, a low power look ahead clock gating is presented and compared it with the previously clock gating technique i.e. the data driven clock gating. This look ahead clock gating has been shown to be very useful in reducing the power. One of the major sources responsible for power consumption in digital circuits is the systems clock signal. It contributes towards a large amount of power consumption. Look ahead clock gating has been shown to be very useful in reducing the power consumed by digital systems. As this look ahead clock gating computing the clock enabling signals of each flip flop one cycle ahead of time, based on the present cycle data of the flip flop on which it depends,

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the drawbacks of the previously three gating methods have been overcome. The tight timing constraints existing in the auto gated flip flop and data driven clock gating methods has been avoided using this look ahead clock gating.

The look ahead clock gating has compared with the data driven clock gating method. The data driven clock gating method shows more power consumption than the look ahead clock gating method. The result shows minimum power consumption than that of data driven clock gating.

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